<center>**REMARKS/ARGUMENTS**</center>

In the Office Action mailed May 7, 2010, claims 1-6 were rejected. In response, Applicant hereby requests reconsideration of the application in view of the amendments and the below-provided remarks. No claims are amended or canceled.

For reference, claims 7-11 are added. In particular, claim 7 is added to recite that the asynchronous processor does not receive and is not dependent on any clock signal. Claim 10 is added to recite similar limitations within the context of the method. These claims are supported, for example, by the subject matter described in the specification at page 4, lines 5-18. Claim 8 is added to recite that the asynchronous processor does not consume power in the absence of receiving the error signal. Claim 11 is added to recite similar limitations within the context of the method. These claims are supported, for example, by the subject matter described in the specification at page 5, lines 14-25. Claim 9 is added to recite limitations similar to the language of claim 2, although within the context of the method. This claim is supported by the original language of the claims.

<u>Claim Rejections under 35 U.S.C. 102 and 103</u>

Claims 1-6 were rejected based on one or more cited references. The cited reference(s) relied on in these rejections include:

Starr et al. (U.S. Pat. No. 6,891,401, hereinafter Starr)

Pohlmeyer et al. (U.S. Pat. No. 6,959,014, hereinafter Pohlmeyer)

In particular, claims 1-4 and 6 were rejected under 35 U.S.C. 102(e) as being anticipated by Starr. Claim 5 was rejected under 35 U.S.C. 103(a) as being unpatentable over Starr in view of Pohlmeyer. However, Applicant respectfully submits that these claims are patentable over Starr and Pohlmeyer for the reasons provided below.

<u>Independent Claim 1</u>

Claim 1 is patentable over Starr because Starr does not disclose all of the limitations of the claim. Claim 1 recites:

An electronic circuit arrangement comprising:
    a clock fail circuit arranged to receive a clock signal and to generate an error signal upon an absence of the clock signal; and
    an asynchronous processor arranged to receive said error signal and to bring the electronic circuit arrangement into a pre-defined state upon detection of the error signal, wherein the asynchronous processor remains dormant in the absence of a clock failure event.
(Emphasis added.)

In contrast, Starr does not disclose all of the limitations of the claim. In particular, Starr does not disclose an asynchronous processor. Furthermore, even if Starr were to disclose an asynchronous processor, generally, Starr does not specifically disclose an asynchronous processor which remains dormant in the absence of a clock failure event.

Starr does not disclose an asynchronous process because the switchover circuit 14 of Starr is not asynchronous. Rather, Starr explicitly describes the switchover circuit 14 operates based on a clock signal. Starr explains that one of the two clock signals is provided for running the switchover circuit 14. Starr, col. 2, lines 58-61; col. 3, lines 11-14. By operating based on a clock signal, the switchover circuit 14 should not be characterized as an asynchronous circuit or processor at least because the clock signal provides a synchronous signal for operating the switchover circuit 14. Therefore, Starr does not disclose an asynchronous processor.

Starr does not disclose an asynchronous processor which remains dormant in the absence of a clock failure event because the switchover circuit 14 of Starr is not dormant in the absence of a clock failure event. Rather, the switchover circuit 14 of Starr remains active so long as the secondary clock signal is supplied to the switchover circuit 14. Specifically, Starr explains that the switchover circuit 14 is only inactivated if the secondary clock signal is lost. Starr, col. 3, lines 14-17. This means that the switchover circuit 14 is active (i.e., not dormant) so long as the secondary clock signal is supplied to the switchover circuit 14, which occurs even while the primary clock signal is active and operating correctly. Therefore, Starr does not disclose an asynchronous processor which remains dormant in the absence of a clock failure event.

For the reasons presented above, Starr does not disclose all of the limitations of the claim because Starr does not disclose an asynchronous processor which remains dormant in the absence of a clock failure event, as recited in the claim. Accordingly, Applicant respectfully asserts claim 1 is patentable over Starr because Starr does not disclose all of the limitations of the claim.

Independent Claim 6

Applicant respectfully asserts independent claim 6 is patentable over the cited reference at least for similar reasons to those stated above in regard to the rejection of independent claim 1. Claim 6 recites subject matter which is similar to the subject matter of claim 1 discussed above. Although the language of this claim differs from the language of claim 1, and the scope of each claim should be interpreted independently of other claims, Applicant respectfully asserts that the remarks provided above in regard to the rejection of claim 1 also apply to the rejection of claim 6.

Dependent Claims

Claims 2-5 and 7-11 depend from and incorporate all of the limitations of the corresponding independent claims 1 and 6. Applicant respectfully asserts these dependent claims are allowable based on allowable base claims. Additionally, each of these dependent claims may be allowable for further reasons.

CONCLUSION

Applicant respectfully requests reconsideration of the claims in view of the amendments and the remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-4019** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-4019** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

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